Remarks:

Reconsideration of the application is respectfully requested.

Claims 1 - 4 and 6 - 17 and 19 - 29 are presently pending in the application. Claim 16 has been amended. Claim 18 has been canceled. New claim 29 has been added.

Applicant gratefully acknowledges that claims 7, 8, 18, 19, 22 - 23 and 25 - 28 have been indicated as being allowable if rewritten to include all the limitations of the claims from which those claims depend. Claim 16 has been amended to include the limitations of former claim 18, thus rendering claim 16 allowable, pursuant to item 3 of the Office Action. Further, new claim 29 includes all of the limitations of former claims 16 and 19, thus rendering claim 29 allowable, pursuant to item 3 of the Office Action. In light of the below arguments setting forth the patentability of claims 1, 11 and 24 over the cited art, Applicant respectfully believes that rewriting of claims 7 - 8, 22 - 23 and 25 - 28 is unnecessary at this time.

In item 2 of the above-identified Office Action, claims 1 - 4, 6, 9 - 17 and 20 - 24 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U. S. Patent No. 6,651,202 to Phan ("**PHAN**").

Applicant respectfully traverses the above rejections.

More particularly, Applicant's independent claim 1 recites, a method of testing an integrated circuit, which comprises:

> providing an integrated circuit that includes a self-test device;
>
> starting to perform a test of the integrated circuit with the self-test device;
>
> taking at least parts of the integrated circuit out of operation after the parts have been tested by the self-test device; and
>
> **subsequently, connecting the integrated circuit to an external testing device** that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test. [emphasis added by Applicant]

As such, Applicant's invention of claim 1 requires, among other things, **starting a test** of the integrated circuit **before connecting the integrated circuit to an external testing device**. This is indicated by the term "**subsequently**" used in the last paragraph of claim 1.

Similarly, Applicant's independent claim 11 recites, an apparatus for testing an integrated circuit using a self-test device that is located in the integrated circuit, which comprises:

> a self-test control device for **causing testing of the integrated circuit by the self-test device before the integrated circuit is connected to an external testing**

> **device** that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test. [emphasis added by Applicant]

Applicant's claims 1 and 11 are supported, for example, in paragraphs [0014] and [006] of the instant application, the latter of which states:

> In the example considered, **the test of the integrated circuit by the BIST module contained therein is begun before the integrated circuit is connected to the external testing device**, for example, as early as during temporary storage of the relevant integrated circuit and/or during the transport of the relevant integrated circuit to the external testing device. The test of the integrated circuit by the BIST module contained therein has preferably already been concluded when the integrated circuit is connected to the external testing device. [emphasis added by Applicant]

At least one advantage of starting the testing of the integrated circuit prior to connection to the external test device is discussed in paragraphs [0068] - [0069] of the instant application, which state:

> Since the external testing device does not itself have to perform the initiation of the test to be carried out by the BIST module, and does not then have to wait until the end of this test before it can begin with reading out and evaluating the results of the test carried out by the BIST module and/or continue testing of the integrated circuit to be tested, **the residence time of the integrated circuit to be tested on the external testing device is minimal**, and the utilization of the external testing device is optimal.
>
> Shortening the residence time of the integrated circuit to be tested on the external testing device may appear to be unimportant. However, if one takes account of

> the immense number of integrated circuits which have to be tested by the external testing device over the course of time, then, even if only a fraction of a second can be saved on each integrated circuit, **the result is an enormous saving in time**. [emphasis added by Applicant]

The **PHAN** reference neither teaches, nor suggests, **subsequently** (i.e., after testing has begun) connecting the integrated circuit to an external tester, i.e. the **external ATE** (Automated Test Equipment) in **PHAN**, as required by Applicant's independent claims 1 and 11. In fact, **PHAN** specifically teaches the opposite. **PHAN** teaches that the built-in self test circuit (BIST/BISR 122 of Fig. 1 of **PHAN**) **must be connected to the external test device (i.e., ATE 160) to operate**. This is taught in col. 2 of **PHAN**, lines 32 - 36, which states:

> In the BIST approach, a test pattern generator and test response analyzer are incorporated directly into the device to be tested. **BIST operation is controlled by supplying an external clock** and via use of a simple commencement protocol. [emphasis added by Applicant]

Further, **PHAN** specifically teaches that the **external clock controlling BIST operation is supplied by the external test device** (i.e., ATE 160 of Fig. 1 of **PHAN**). More particularly, col. 8 of **PHAN**, lines 5 - 18, states:

> The integrated circuit IC further includes BIST/BISR circuitry 122 such as that shown in FIG. 1. The BIST/BISR circuitry 122 interfaces with an embedded memory array 100 as previously described, and also communicates with the external ATE 160 via the register

> output FLARESCAN_OUT or similar means. The register output signal FLARESCAN_OUT provides the external ATE 200 with addresses of memory locations of the embedded memory array 100 which fail BIST analysis.
>
> In the disclosed embodiment of the invention, **clocking of the BIST/BISR circuitry 122 is controlled by a clock signal FLARESCAN_IN_CLK from the external ATE 160. Other control signals may also be communicated as necessary from the external ATE 160 to the BIST/BISR circuitry 122.** [emphasis added by Applicant]

As such, **PHAN** specifically teaches that for operation of the self test circuit, **the external test device ATE is connected to, and provides, at the very least, the clock signals that control the operation of the self test circuitry BIST/BISR.**

As such, **PHAN** specifically teaches that the **BIST** self test operation must be operated using an external clock **provided by the external test equipment ATE.** The BIST/BISR self test circuitry of **PHAN**, having no clock signal of its own, **does not start the testing of the integrated circuit prior to connection with the external test device ATE, as required by Applicant's claims 1 and 11.**

In view of the foregoing, it is believed that Applicant's claims 1 and 11 are patentable over the **PHAN** reference.

Further, Applicant's independent claim 24 recites, a wafer comprising:

> a plurality of integrated circuits that are configured for being separated apart by a subsequent cutting process;
>
> each of said plurality of integrated circuits including a self-test device located in said integrated circuit;
>
> **said plurality of said integrated circuits are at least partially electrically connected to one another.** [emphasis added by Applicant]

As such, on Applicant's wafer of claim 24, the plurality of integrated circuits are **at least partially electrically connected to one another.** This feature of Applicant's claim 24 is neither taught, nor suggested, in **PHAN.** As pointed out in the Office Action, col. 10 of **PHAN**, lines 35 - 39, states:

> It will also be appreciated that execution of the BIST/BISR routines in steps 204 and 210 may be performed both prior to and following singulation and packaging of the integrated circuit IC from the other die of the semiconductor wafer.

See also, col. 3 of **PHAN**, lines 36 - 39. However, nothing in the cited portion of **PHAN**, or anywhere else in **PHAN**, specifically teaches or suggests that the integrated circuit under test is **at least partially electrically connected to any other integrated circuit on a wafer**, as required by Applicant's claim 24. Rather, it can be concluded from the portion of **PHAN** cited in the Office Action, that **each integrated circuit is tested individually from the other integrated circuits on the wafer** (i.e., the voltages or

signals required for testing are fed individually to teach of the integrated circuits to be tested). For example, the portion of **PHAN** cited in the Office Action indicates that the " . . .**BIST/BISR** routines in steps 204 and 210 **may be performed** both prior to and following singulation and packaging **of the integrated circuit IC from the other die of the semiconductor wafer.**" (i.e., the BIST/BISR routines being performed on "**the**" integrated circuit IC, and not simultaneously on "the other die" of the wafer). As such, it would appear from **PHAN** that the testing of "**the**" **(i.e., "an")** integrated circuit IC occurs individually, despite plural ICs being located on a wafer.

In view of the foregoing, it is believed that **PHAN** fails to teach or suggest, among other limitations of Applicant's claims, **the plurality of integrated circuits being at least partially electrically connected to one another**, as required by Applicant's claim 24. Therefore, claim 24 is believed to be patentable over the **PHAN** reference.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1, 11, 16 and 24. Claims 1, 11, 16 and 24 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well

because they all are ultimately dependent on claims 1, 11, 16 or 24.

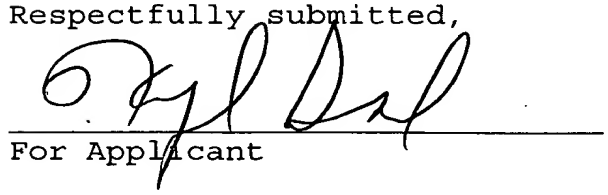
In view of the foregoing, reconsideration and allowance of claims 1 - 4 and 6 - 17 and 19 - 29 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



Kerry P. Sisselman
Reg. No. 37,237

For Applicant

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Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101